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Apalis Computer Module

Module Specification

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27th November 2015	V1.6	Section 2.4: Added details for Apalis iMX6 module.
4th January 2021	V1.7	Section 2.4: Added Apalis TK1, Apalis iMX8, and Apalis iMX8X modules Section 3.2.1: Clarify position of JTAG pads and update figure 7 Section 4.4: Update figure 10 and 11 Section 5.1: Clarify maximum current draw Update Disclaimer Minor changes
21st February 2022	V1.8	Eliminating section 2.4 as it is replicating information already contained within SoM datasheets Minor changes

Contents

1. Introduction

1.1 Overview

This document is a specification which defines the Apalis® Computer-on-Module (referred to hereafter as “module”). It defines the interfaces in terms of functional and electrical characteristics, signal definitions and pin assignments. It also defines the mechanical form factor, including key dimensions.

1.2 Motivations

The following motivations are central to the definition of the new Apalis® module specification. **It should be clearly noted that the Apalis® computer module family is not a replacement for the Colibri computer module family.** Both are very complementary to one another, and whilst may overlap in terms of suitability for some specific applications, they differ significantly in a variety of areas including, but not limited to, size, features and cost.

1. As ARM based SoC (System-on-Chip) technology continues to evolve, support for a wider range of interfaces is being added, such as PCI-express, Gigabit Ethernet, HDMI, etc. The Apalis® module will enable customers to benefit from these evolutions. It should also be noted that nothing in the module specification restricts any Apalis® based products from using non-ARM architectures. In this respect, the specification is very architecture independent.

2. With the recent advancements in ARM based SoC technology, including but not limited to the addition of a wider variety of high speed interfaces and the huge advancement in graphics capability, such as 2D/3D hardware acceleration, full HD rendering and multiple display support, it is possible to access markets previously reserved for higher power, x86 based technologies, such as the Intel Atom. The Apalis® module will provide a platform with which to enable this technology to compete in these application areas and address the shortcomings of existing x86 based products.

3. As the pace in performance advancement is accelerating faster than the increase in performance efficiency, we are seeing an increasing trend in power consumption in high performance ARM based SoCs. Whilst passive cooling is still perfectly viable in many applications, this increase in power consumption means that allowances for additional cooling solutions, such as heat spreaders for conduction cooling, must be made. The Apalis® module provides a robust, rigid mounting mechanism to support such thermal solutions.

4. The Apalis® module has been developed from in depth research into different technologies, rather than a specific SoC. This will help to future proof the Apalis® module architecture whilst making it suitable for supporting a wide range of SoCs.

5. The Apalis® module encapsulates the complexity associated with modern day electronic design, such as high speed impedance controlled layouts with high component density utilising blind and buried via technology. This allows the customer to create a carrier board which implements the application specific electronics which is generally much less complicated. The Apalis® module takes this one step further and implements an interface pin out which allows direct connection of real world I/O ports without needing to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high speed, serial technologies that use impedance controlled differential pairs, as it allows them to easily route such interfaces to common connectors in a simple, robust fashion.

2. Module Overview

2.1 Architecture

The block diagram in figure 1 shows the basic architecture of the Apalis® module, depicting the standard interfaces and some examples of type-specific interfaces.

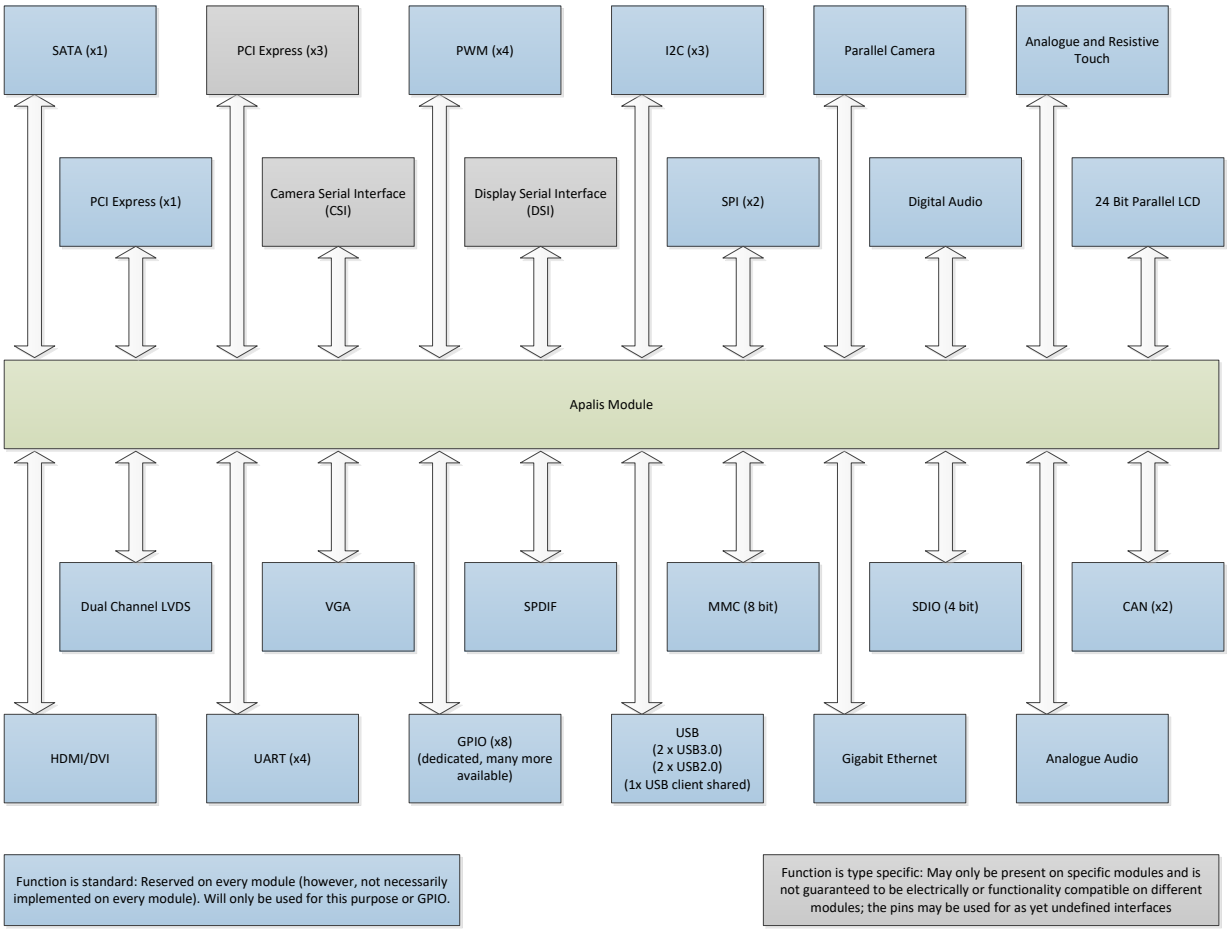

Figure 1: Apalis® Module Architecture

2.2 Features

Features of the Apalis® module are split into two distinct groups: *standard* and *type-specific*.

Standard features are features that are allocated for use on every Apalis® module. Although they may not be fully supported or implemented on every module, pins are reserved specifically for them and shall not be used for any other purpose in the future. This guarantees electrical compatibility between designs which only make use of standard features, helping to ensure carrier board design longevity and support for future module designs.

A type-specific feature is a feature which is not guaranteed to be functionality or electrically compatible between modules. If a carrier board design uses such features, then it is possible that other modules in the Apalis® module family do not provide these features and instead provide other features on the associated pins. In this case, Apalis® modules which are suitable for use in the carrier board design may be restricted.

2.3 Interface Summary

This section provides a list of interfaces that are defined as standard, and some examples of those interfaces which may be type-specific.

2.3.1 Standard Interfaces

By dedicating specific pins for specific functions, the Apalis® module family is able to ensure electrical and functional compatibility between module family members, helping future proof designs against advances in technology and providing an upgrade path for products, decoupling the product from reliance on a specific device or device family. Every effort shall be taken to maintain functional compatibility between module family members where it commercially and technically viable.

The table in figure 2 shows the standard interfaces that are provided by an Apalis® module. The “GPIO Capable” column indicates whether, for a specific interface, the assigned pins can be used as GPIOs. Yes and No are self-explanatory, Optional indicates that it may be possible for some modules, but not all.

The “Standard” column indicates the number of interfaces that the specification allows for in the standard pin out. Customers should consult the datasheet for specific Apalis® module variants to check which interfaces are available for that module.

Description	Standard	Note	GPIO Capable
4/5 Wire Resistive Touch	1	Touch wiper shared with analogue input 4	No
Analogue Inputs	4	Minimum 8 bit resolution, 0-3.3V nominal range	No
Analogue Audio	1	Line in L&R, Microphone in, Headphone out L&R	No
CAN	2		Optional
Digital Audio	1	I^2S	Yes
Dual Channel LVDS Display	1	1x or 2x single channel or 1x dual channel mode	No
Gigabit Ethernet	1		No
GPIO	8		Yes
HDMI (TDMS)	1		No
I2C	3	Including DDC	Yes
Parallel Camera	1	8 bit YUV	Optional
Parallel LCD	1	24 bit resolution	Optional
PCI-Express (lane count)	1	Single lane and clock	No
PWM	4		Yes
SATA	1		No
SDIO	1	4 bit	Yes
SDMMC	1	8 bit	Yes
S/PDIF	1	1 input, 1 output	Optional
SPI	2		Yes
UART	4	1 Full Function, 1 CTS/RTS, 2 RXD/TXD only	Yes
USB	4	2 x USB 3.0, 2 x USB 2.0, 1 x shared host/client USB 2.0	No
VGA	1		No

Figure 2: Standard Interfaces

2.3.2 Type-Specific Interfaces

Type-specific interfaces allow for the possibility of including interfaces which may not yet exist or be widely adopted, or interfaces which may be specific to a particular device or groups of devices. They also offer a mechanism of extending features which are present on the standard interfaces, such as providing additional PCI-Express lanes. This provides the Apalis® module with the flexibility of being able to reconfigure a subset of pins for different uses between different modules.

It should be noted that type-specific interfaces will be kept common across modules that share such interfaces where possible. For example, if both module A and module B have three additional PCI-Express lanes which are available in the same configurations as a type-specific interface, then they shall be assigned to the same pins in the type-specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type-specific interface.

2.4 Module and Carrier Board Compatibility

To ensure any carrier board design is 100% compatible with all Apalis® modules, only the standard interfaces should be used.

If a custom carrier board design uses any type-specific interfaces, then it may not be 100% compatible with all Apalis® modules. Where type-specific interfaces are common between different Apalis® modules, they shall be provided on the same pins where possible. Therefore, designs that make use of the type-specific interfaces of a specific Apalis® module may be compatible with other Apalis® modules – please check the interface specifications of individual Apalis® modules carefully.

2.5 Connector

The Apalis® module is based around the MXM3 (Mobile PCI-Express Module) edge connector. This connector has been adopted by various manufacturers for use in the embedded COM market and, based on the range of connectors available on the market at the current time, is the only suitable connector based on the Apalis® module requirements.

A picture of the MXM3 connector can be found in figure 4.

Figure 4: An MXM3 edge connector

The connector provides a total of 310 usable contacts. A large proportion of the contacts are reserved for the standard interfaces, whilst a smaller subset is reserved for type-specific interfaces.

The recommended connector for the Apalis® module is the JAE MM70-314-310B1, which has a board height of 3.0mm.

2.6 MXM SnapLock™

The Apalis® module can be fixed easily to the carrier board using either M3 screws or a unique connector mechanism called MXM SnapLock™. MXM SnapLock™ uses an edge retention connector which is mounted on the carrier board and retains the Apalis® module in place using two metal retaining clips and locating pips. For many applications and during development, this provides a simple retention mechanism.

For applications where the system is likely to experience a high level of vibration or harshness, a set of M3 bolts combined with SMT aluminium stand-offs mounted in the carrier board can be used.

3. Interface Specifications

3.1 Signal Naming Convention

Where there are multiple signals of the same type which are part of a group and are identified by a suffix index (e.g. PWM1, PWM2, etc.), then the index always starts with a one (as opposed to a zero). For signals which are named after a standard or follow a widely acknowledged common naming convention (such as the Ethernet or LVDS interfaces), they may use a zero based index.

Differential pair signal components are suffixed with either a "+" or "-". Active low signals are suffixed with a "#".

The underscore ("_") is used as a separator to split component parts of the signal name (such as signal group, channel and signal descriptor components) to make the signal name easy to read and interpret.

3.2 Signal Definition

This section contains detailed information on the signals provided by the Apalis® module, such as signal class and voltage domains. Please refer to the key in figure 5 for the various voltage domain definitions.

Only those voltage domains marked in green are required to be supplied externally for module operation, and those in orange are optional.

The domains that are not marked in green or orange are not required to be supplied to the module.

Some of the voltage domains specified are used purely to indicate power supply tolerances on pins which are specified to operate on that domain. Hence, they are not necessarily power supplies that are generated by the module nor required by the module.

Voltage Domain	Nominal Value	Absolute Maximum Value	Definition
VCC	3.3V	3.5V	Main system power supply from carrier board.
VCC_IO	3.3V	3.5V	Multi-purpose I/O.
VCC_BACKUP	3.3V	3.5V	Backup supply for features such as Real-Time Clock (RTC)
VCC_ETH	TBD	TBD	Ethernet centre tap power supply. Controller dependent and output only.
VCC_USB	5.0V	5.5V	USB bus power supply.
VCC_HDMI	5.0V	5.5V	Hot plug detected voltage from connector display.
AVCC	3.3V	3.5V	Analogue power supply from carrier board.
AVCC_IO	3.3V	3.5V	Analogue I/O.

Figure 5: Voltage Domain Definitions

Check carefully in individual signal definitions to determine the voltage domain to which a signal belongs. Do not assume that a signal which shares a group or class name with a voltage domain is automatically on that voltage domain. For instance, the VCC_HDMI voltage domain is applicable for supply voltage and control signals, but not for the differential mode signals.

3.2.1 JTAG and Generic Test Point Interfaces

Every Apalis® module provides a series of 20 test points; 10 along the left side and 10 along the right side of the bottom of the module PCB as shown in figure 7. Each set of test points is symmetrical about the centred Y-axis (the Y plane is orthogonal to the connector edge).

These test points shall provide access to any JTAG interface that is supported by the module (this is normally the JTAG interface as provided by the SoC) as well as module specific signals, generally for the purposes of measurement.

The JTAG interface pins are always the topmost 7 pins on the right edge of the module when the module is viewed from the bottom side. These test points are always reserved for the JTAG interface and will never provide any other signals. They are depicted by green primitives in figure 7.

The remaining 13 test points are module specific pins. The signals connected to these test points are defined in the datasheet for each individual Apalis® module. They are depicted by orange primitives in figure 7.

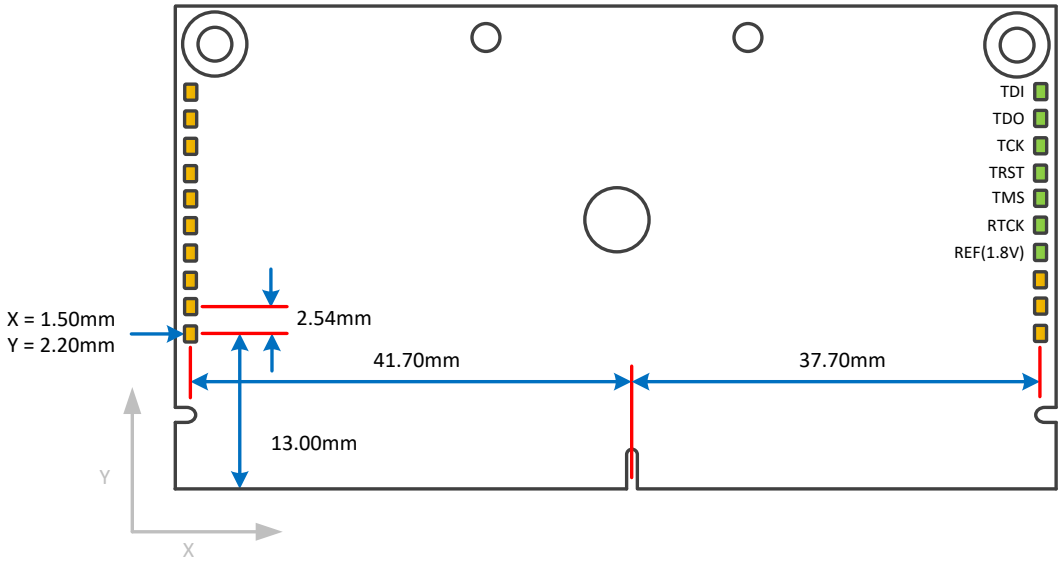

Figure 7: Bottom side of module illustrating test points and relative positions (bottom view)

3.3 Parallel LCD

The parallel LCD interface is a 24 bit interface. The signals are defined in groups of pins assigned to the Red, Green and Blue, with R7, G7 and B7 being the Most Significant Bits (MSBs) and R0, G0 and B0 being the Least Significant Bits (LSBs) for the respective colours. To ensure compatibility between modules, the display interface should always be used in 24 bit mode. To use displays which require fewer bits (e.g. 18 or 16 bit displays), simply do not connect the bottom n LSBs for each colour, where n is the number of signals that are not required for a specific colour. For instance, to connect an 18 bit display, R0, R1, G0, G1 B0 and B1 will remain unused, and R2, G2 and B2 become the LSBs for this configuration. More detailed information regarding configuration shall be provided in the reference design guide.

3.4 Parallel Camera

For compatibility between modules, the parallel camera interface shall normally be configured by default to operate in 8 bit YUV mode. Modules may support other modes with greater bit depths; in such cases, additional pins will be made available as type-specific interfaces as necessary, and compatibility between different modules for such modes cannot be guaranteed.

3.5 Physical Pin Definition and Location

Signal definitions in terms of physical pins and their locations on the Apalis® module can be found in the appendix. The table in appendix C defines the physical pins and their location on the Apalis® module. This definition also includes missing pins (marked with a grey cell) to represent the physical space on the connector where these pins are missing.

The total number of usable pins on the module is 310. The ground pin count is 41 (~13%). The main power supply (VCC) power pin count is 10.

3.6 Direct Breakout™

Direct Breakout™ aims to reduce complexity of carrier board routing from the module connector to the real world I/O ports by making it possible to route signals without requiring any trace gathering or cross over for critical

signals. This is achieved by taking care of the complexity of routing high speed, impedance critical signals from the source IC to the edge connector on the Apalis® module. I/O is generally gathered into functional “rooms” on the connector so that all signals associated with a specific interface are in one place, reducing routing complexity.

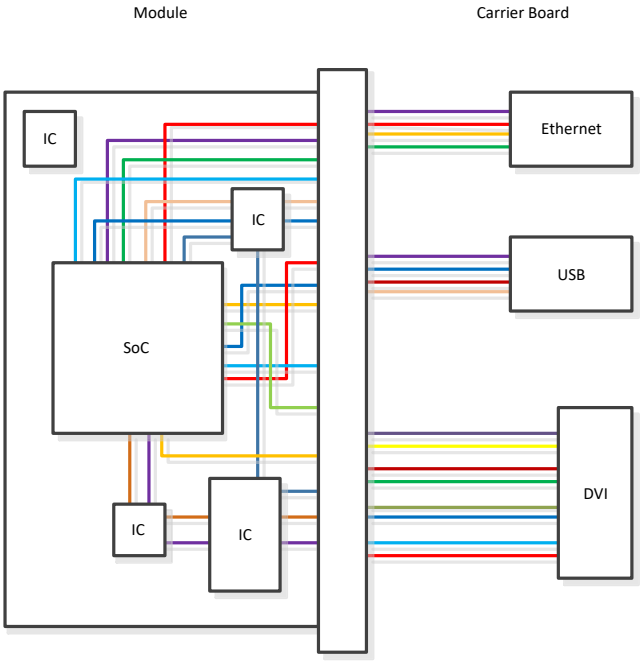

Figure 8: Direct Breakout Example

The image in figure 8 shows the concept of direct breakout by illustrating how complex routing and layout is encapsulated on the Apalis® module, providing the potential for simple routing on the carrier board.

4. Mechanical Specifications

4.1 Overview

The Apalis® module form factor mechanical dimensions have been specified based on careful analysis of required board space for typical device packages (e.g. 23mm x 23mm 0.8mm pitch SoC, 4 x16 memory ICs, power ICs and peripheral ICs) and certain key features (e.g. as dual channel [2 x 32bit] memory bus). This has been balanced with the requirement to keep the form factor as small as is reasonably possible. A single mechanical size has been defined.

4.2 Mounting and Fixation

MXM SnapLock™ or M3 screws in combination with threaded standoffs shall be used to fasten the module to the carrier board. A keep out area on the bottom side of the module located in the centre is reserved to allow a mechanical standoff on the carrier board to come into contact with the PCB when the module is fully inserted. This will allow pressure to be placed on the top side of the module which may be required for thermal cooling solutions without exerting a bending moment on the PCB. Carrier board design requirements shall be detailed in a separate carrier board design guide application note.

4.3 Module Size

4.3.1 Width, Length, Height and Key Primitives

Figure 9 shows a mechanical drawing of the outline of the Apalis® module together with key dimensions.

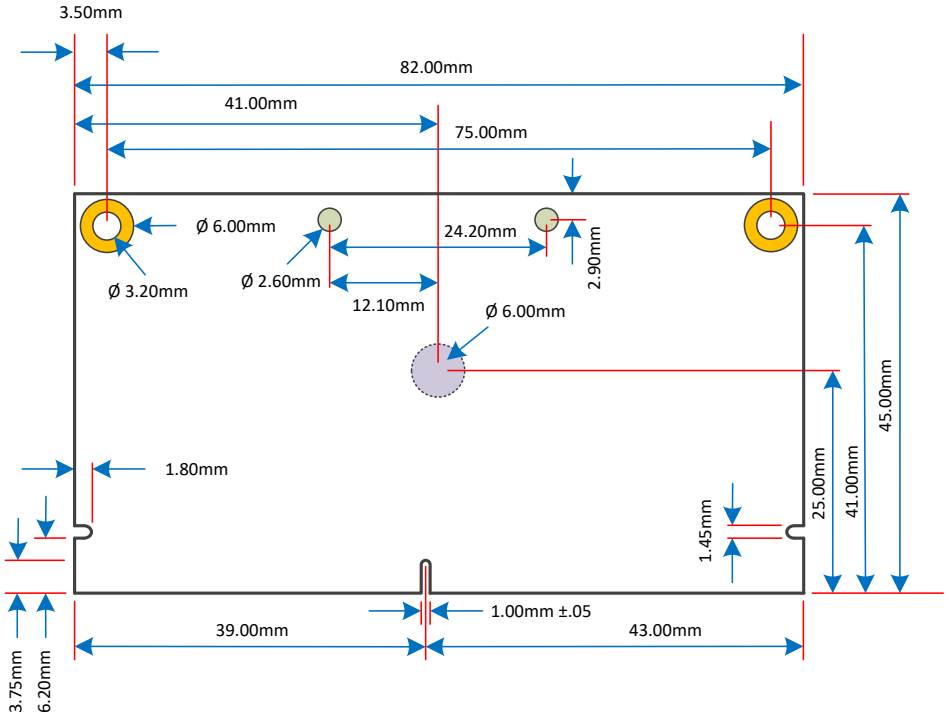

Figure 9: Apalis® Module Mechanical Dimensions Top View

The Apalis® module extends in the Y plane (the plane which is orthogonal to the connector edge) for 45mm from one PCB edge to the other.

The thickness of the Apalis® module PCB is 1.2mm. The maximum component height on the bottom side of the Apalis® module shall be limited to 1.8mm. With the recommended MXM connector (P/N: JAE MM70-314-310B1), the component height on the carrier board directly underneath the Apalis® module should not exceed 1.0mm.

4.4 Pin Numbering

The diagrams in figures 10 and 11 show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema.

Pins on the top side of the module have an even number and pins on the bottom side have an odd number.

The pin number increases linearly as a multiple of the pitch – that is, pins which are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins which do not exist due to the connector notch are also accounted for (pins 166 through 172).

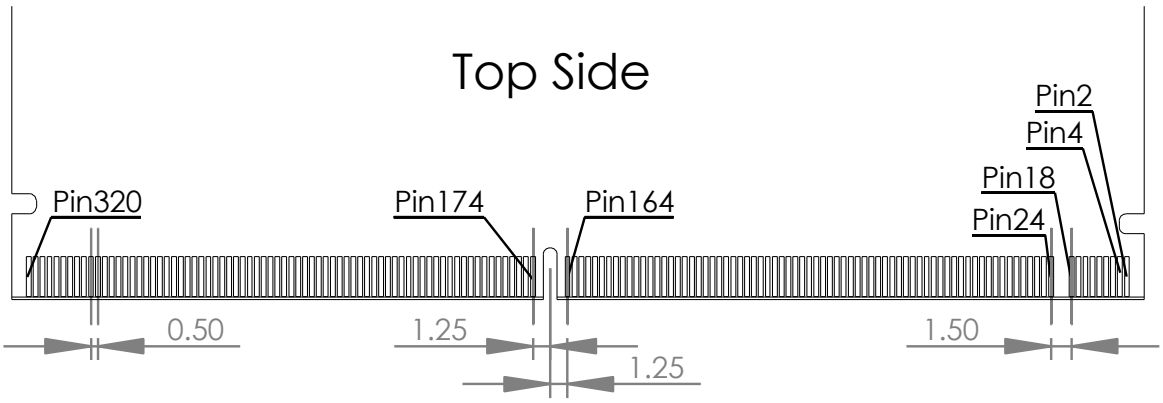

Figure 10: Pin numbering schema on the top side of the module

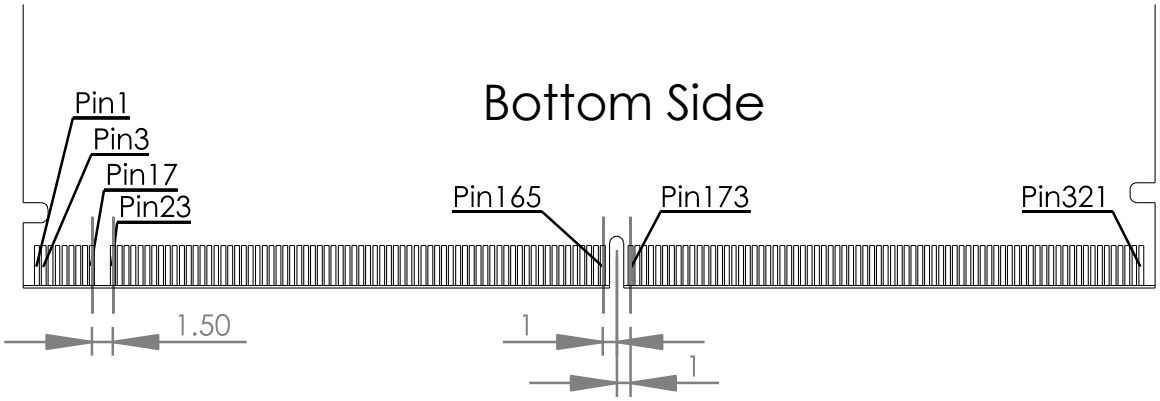

Figure 11: Pin numbering schema on the bottom side of the module

5. Electrical Specifications

5.1 Power Supplies

All Apalis® modules are capable of being powered with a single main power supply powering VCC and AVCC, and if required, a low current backup power supply for purposes such as Real Time Clock (RTC) support. To minimise the impact of noise on the sensitive analogue parts of the system, it is highly recommended that VCC and AVCC be supplied through independent power supplies (for instance, AVCC can be generated via an LDO due to its low current requirements).

Based on the power supply rating of the connector pins and the number of pins assigned as main (VCC) power supply pins, the maximum continuous current draw from VCC is 5 amps. Some modules might require delivering higher peak current values.

Further carrier board power supply requirements in terms of power rating, isolation and decoupling, bulk capacitance, and characteristics such as ramp up rate, etc. are detailed in a separate carrier board design guide document.

5.2 Power Control

There are no power control features built into the module from the power on/power off perspective. If a specific implementation requires a power on button, then it shall be the responsibility of the carrier board to implement this functionality.

VCC and AVCC are the two minimum power supplies which are required to be present for the module to become operational. Once VCC is present and is within specification, then the module will power up and start normal operation automatically.

VCC_BACKUP is not required for the module to start normal operation, however, it is permanently required if the application requires features which rely on this supply being always on, such as the Real-Time Clock (RTC).

5.3 Back Feed Protection

Protection from back feeding from devices on the carrier board can be achieved using the signal “POWER_ENABLE_MOCI”. This signal will be asserted by the module to indicate that the carrier board can power up any external devices (such as signal transceivers, converters, level shifters, secondary MPUs, etc.) which may otherwise cause undesired back feeding prior to and during the module power up process. Detailed information on the use of this signal shall be provided in a separate carrier board design guide application note.

6. Appendix A – Module Top Side Signal Definition

Pin Number	Signal Group	Signal Name	Signal Class	Voltage Domain
2	PWM	PWM1	Output	VCC_IO
4		PWM2	Output	VCC_IO
6		PWM3	Output	VCC_IO
8		PWM4	Output	VCC_IO
10	CAN	VCC	Power	VCC
12		CAN1_RX	Input	VCC_IO
14		CAN1_TX	Output	VCC_IO
16		CAN2_RX	Input	VCC_IO
18		CAN2_TX	Output	VCC_IO
24	System Control	POWER_ENABLE_MOCI	Output	VCC_IO
26		RESET_MOCI#	Output	VCC_IO
28		RESET_MICO#	Input	VCC_IO
30	Gigabit Ethernet	VCC	Power	VCC
32		ETH1_MDI2+	Differential Pair	N/A
34		ETH1_MDI2-	Differential Pair	N/A
36		VCC	Power	VCC
38		ETH1_MDI3+	Differential Pair	N/A
40		ETH1_MDI3-	Differential Pair	N/A
42		ETH1_ACT	Output	VCC_IO
44		ETH1_LINK	Output	VCC_IO
46		ETH1_CTREF	Analogue Output	VCC_ETH
48		ETH1_MDI0-	Differential Pair	N/A
50		ETH1_MDI0+	Differential Pair	N/A
52		VCC	Power	VCC
54		ETH1_MDI1-	Differential Pair	N/A
56		ETH1_MDI1+	Differential Pair	N/A
58	USB*	VCC	Power	VCC
60		USBO1_VBUS	Input	VCC_USB
62		USBO1_SSRX+	Differential Pair	N/A
64		USBO1_SSRX-	Differential Pair	N/A
66		VCC	Power	VCC
68		USBO1_SSTX+	Differential Pair	N/A
70		USBO1_SSTX-	Differential Pair	N/A
72		USBO1_ID	Input	VCC_IO
74		USBO1_D+	Differential Pair	N/A
76		USBO1_D-	Differential Pair	N/A
78		VCC	Power	VCC
80		USBH2_D+	Differential Pair	N/A
82		USBH2_D-	Differential Pair	N/A
84		USBH_EN	Output	VCC_IO
86		USBH3_D+	Differential Pair	N/A
88		USBH3_D-	Differential Pair	N/A
90		VCC	Power	VCC
92		USBH4_SSRX-	Differential Pair	N/A
94		USBH4_SSRX+	Differential Pair	N/A
96		USBH_OC#	Input	VCC_IO
98		USBH4_D+	Differential Pair	N/A
100		USBH4_D-	Differential Pair	N/A
102		VCC	Power	VCC
104		USBH4_SSTX-	Differential Pair	N/A
106		USBH4_SSTX+	Differential Pair	N/A
108	UART	VCC	Power	VCC
110		UART1_DTR	Output	VCC_IO
112		UART1_TXD	Output	VCC_IO

114		UART1_RTS	Output	VCC_IO
116		UART1_CTS	Input	VCC_IO
118		UART1_RXD	Input	VCC_IO
120		UART1_DSR	Input	VCC_IO
122		UART1_RI	Input	VCC_IO
124		UART1_DCD	Input	VCC_IO
126		UART2_TXD	Output	VCC_IO
128		UART2_RTS	Output	VCC_IO
130		UART2_CTS	Input	VCC_IO
132		UART2_RXD	Input	VCC_IO
134		UART3_TXD	Output	VCC_IO
136		UART3_RXD	Input	VCC_IO
138		UART4_TXD	Output	VCC_IO
140		UART4_RXD	Input	VCC_IO
142	MMC	GND	Power	GND
144		MMC1_D2	Bidirectional	VCC_IO
146		MMC1_D3	Bidirectional	VCC_IO
148		MMC1_D4	Bidirectional	VCC_IO
150		MMC1_CMD	Bidirectional	VCC_IO
152		MMC1_D5	Bidirectional	VCC_IO
154		MMC1_CLK	Output	VCC_IO
156		MMC1_D6	Bidirectional	VCC_IO
158		MMC1_D7	Bidirectional	VCC_IO
160		MMC1_D0	Bidirectional	VCC_IO
162		MMC1_D1	Bidirectional	VCC_IO
164		MMC1_CD#	Input	VCC_IO
174	SDIO	VCC_BACKUP	Power	VCC_BACKUP
176		SD1_D2	Bidirectional	VCC_IO
178		SD1_D3	Bidirectional	VCC_IO
180		SD1_CMD	Bidirectional	VCC_IO
182		GND	Power	GND
184		SD1_CLK	Output	VCC_IO
186		SD1_D0	Bidirectional	VCC_IO
188		SD1_D1	Bidirectional	VCC_IO
190		SD1_CD#	Input	VCC_IO
192	Digital Audio	GND	Power	GND
194		DAP1_MCLK	Output	VCC_IO
196		DAP1_D_OUT	Output	VCC_IO
198		DAP1_RESET#	Output	VCC_IO
200		DAP1_BIT_CLK	Output	VCC_IO
202		DAP1_D_IN	Input	VCC_IO
204		DAP1_SYNC	Output	VCC_IO
206	VGA	GND	Power	GND
208		VGA1_R	Output	N/A
210		VGA1_G	Output	N/A
212		VGA1_B	Output	N/A
214		VGA1_HSYNC	Output	VCC_IO
216		VGA1_VSYNC	Output	VCC_IO
218	HDMI	GND	Power	GND
220		HDMI1_CEC	Bidirectional	VCC_IO
222		HDMI1_TXD2+	Differential Pair	N/A
224		HDMI1_TXD2-	Differential Pair	N/A
226		GND	Power	GND
228		HDMI1_TXD1+	Differential Pair	N/A
230		HDMI1_TXD1-	Differential Pair	N/A
232		HDMI1_HPD	Input	VCC_HDMI
234		HDMI1_TXD0+	Differential Pair	N/A
236		HDMI1_TXD0-	Differential Pair	N/A
238		GND	Power	GND

240		HDMI1_TXC+	Differential Pair	N/A
242		HDMI1_TXC-	Differential Pair	N/A
244	Dual Channel LVDS	GND	Power	GND
246		LVDS1_A_CLK-	Differential Pair	N/A
248		LVDS1_A_CLK+	Differential Pair	N/A
250		GND	Power	GND
252		LVDS1_A_TX0-	Differential Pair	N/A
254		LVDS1_A_TX0+	Differential Pair	N/A
256		GND	Power	GND
258		LVDS1_A_TX1-	Differential Pair	N/A
260		LVDS1_A_TX1+	Differential Pair	N/A
262		USBO1_OC#	Input	VCC_IO
264		LVDS1_A_TX2-	Differential Pair	N/A
266		LVDS1_A_TX2+	Differential Pair	N/A
268		GND	Power	GND
270		LVDS1_A_TX3-	Differential Pair	N/A
272		LVDS1_A_TX3+	Differential Pair	N/A
274		USBO1_EN	Output	VCC_IO
276		LVDS1_B_CLK-	Differential Pair	N/A
278		LVDS1_B_CLK+	Differential Pair	N/A
280		GND	Power	GND
282		LVDS1_B_TX0-	Differential Pair	N/A
284		LVDS1_B_TX0+	Differential Pair	N/A
286		BKL1_ON	Output	VCC_IO
288		LVDS1_B_TX1-	Differential Pair	N/A
290		LVDS1_B_TX1+	Differential Pair	N/A
292		GND	Power	GND
294		LVDS1_B_TX2-	Differential Pair	N/A
296		LVDS1_B_TX2+	Differential Pair	N/A
298		GND	Power	VCC
300		LVDS1_B_TX3-	Differential Pair	N/A
302		LVDS1_B_TX3+	Differential Pair	N/A
304	Analogue Audio	AGND	Power	AGND
306		AAP1_MICIN	Analogue Input	N/A
308		AGND	Power	AGND
310		AAP1_LIN_L	Analogue Input	N/A
312		AAP1_LIN_R	Analogue Input	N/A
314		AVCC	Power	AVCC
316		AAP1_HP_L	Analogue Output	N/A
318		AAP1_HP_R	Analogue Output	N/A
320		AVCC	Power	AVCC

* USBO denotes USB OTG (On-The-Go), USBH denotes USB Host

7. Appendix B - Module Bottom Side Signal Definition

Pin Number	Signal Group	Signal Name	Signal Class	Voltage Domain
1	GPIO	GPIO1	Bidirectional	VCC_IO
3		GPIO2	Bidirectional	VCC_IO
5		GPIO3	Bidirectional	VCC_IO
7		GPIO4	Bidirectional	VCC_IO
9		GND	Power	GND
11		GPIO5	Bidirectional	VCC_IO
13		GPIO6	Bidirectional	VCC_IO
15		GPIO7	Bidirectional	VCC_IO
17		GPIO8	Bidirectional	VCC_IO
23	SATA	GND	Power	GND
25		SATA1_RX+	Differential Pair	N/A
27		SATA1_RX-	Differential Pair	N/A
29		GND	Power	GND
31		SATA1_TX-	Differential Pair	N/A
33		SATA1_TX+	Differential Pair	N/A
35		SATA1_ACT#	Output	VCC_IO
37	PCI-Express	WAKE1_MICO#	Input	VCC_IO
39		GND	Power	GND
41		PCIE1_RX-	Differential Pair	N/A
43		PCIE1_RX+	Differential Pair	N/A
45		GND	Power	GND
47		PCIE1_TX-	Differential Pair	N/A
49		PCIE1_TX+	Differential Pair	N/A
51		GND	Power	GND
53		PCIE1_CLK-	Differential Pair	N/A
55		PCIE1_CLK+	Differential Pair	N/A
57	Reserved for type-specific features	GND	Power	GND
59		TS_DIFF1-	Undefined	Undefined
61		TS_DIFF1+	Undefined	Undefined
63		TS_1	Undefined	Undefined
65		TS_DIFF2-	Undefined	Undefined
67		TS_DIFF2+	Undefined	Undefined
69		GND	Power	GND
71		TS_DIFF3-	Undefined	Undefined
73		TS_DIFF3+	Undefined	Undefined
75		GND	Power	GND
77		TS_DIFF4-	Undefined	Undefined
79		TS_DIFF4+	Undefined	Undefined
81		GND	Power	GND
83		TS_DIFF5-	Undefined	Undefined
85		TS_DIFF5+	Undefined	Undefined
87		TS_2	Undefined	Undefined
89		TS_DIFF6-	Undefined	Undefined
91		TS_DIFF6+	Undefined	Undefined
93		GND	Power	GND
95		TS_DIFF7-	Undefined	Undefined
97		TS_DIFF7+	Undefined	Undefined
99		TS_3	Undefined	Undefined
101		TS_DIFF8-	Undefined	Undefined
103		TS_DIFF8+	Undefined	Undefined
105		GND	Power	GND
107		TS_DIFF9-	Undefined	Undefined
109		TS_DIFF9+	Undefined	Undefined
111		GND	Power	GND
113		TS_DIFF10-	Undefined	Undefined

115		TS_DIFF10+	Undefined	Undefined
117		GND	Power	GND
119		TS_DIFF11-	Undefined	Undefined
121		TS_DIFF11+	Undefined	Undefined
123		TS_4	Undefined	Undefined
125		TS_DIFF12-	Undefined	Undefined
127		TS_DIFF12+	Undefined	Undefined
129		GND	Power	GND
131		TS_DIFF13-	Undefined	Undefined
133		TS_DIFF13+	Undefined	Undefined
135		TS_5	Undefined	Undefined
137		TS_DIFF14-	Undefined	Undefined
139		TS_DIFF14+	Undefined	Undefined
141		GND	Power	GND
143		TS_DIFF15-	Undefined	Undefined
145		TS_DIFF15+	Undefined	Undefined
147		GND	Power	GND
149		TS_DIFF16-	Undefined	Undefined
151		TS_DIFF16+	Undefined	Undefined
153		GND	Power	GND
155		TS_DIFF17-	Undefined	Undefined
157		TS_DIFF17+	Undefined	Undefined
159		TS_6	Undefined	Undefined
161		TS_DIFF18-	Undefined	Undefined
163		TS_DIFF18+	Undefined	Undefined
165		GND	Power	GND
173	Parallel Camera	CAM1_D7	Input	VCC_IO
175		CAM1_D6	Input	VCC_IO
177		CAM1_D5	Input	VCC_IO
179		CAM1_D4	Input	VCC_IO
181		CAM1_D3	Input	VCC_IO
183		CAM1_D2	Input	VCC_IO
185		CAM1_D1	Input	VCC_IO
187		CAM1_D0	Input	VCC_IO
189		GND	Power	GND
191		CAM1_PCLK	Input	VCC_IO
193		CAM1_MCLK	Output	VCC_IO
195		CAM1_VSYNC	Input	VCC_IO
197		CAM1_HSYNC	Input	VCC_IO
199	I2C	GND	Power	GND
201		I2C3_SDA	Bidirectional	VCC_IO
203		I2C3_SCL	Output	VCC_IO
205		I2C2_SDA	Bidirectional	VCC_IO
207		I2C2_SCL	Output	VCC_IO
209		I2C1_SDA	Bidirectional	VCC_IO
211		I2C1_SCL	Output	VCC_IO
213	SPDIF	GND	Power	GND
215		SPDIF1_OUT	Output	VCC_IO
217		SPDIF1_IN	Input	VCC_IO
219	SPI	GND	Power	GND
221		SPI1_CLK	Output	VCC_IO
223		SPI1_MISO	Input	VCC_IO
225		SPI1_MOSI	Output	VCC_IO
227		SPI1_CS	Output	VCC_IO
229		SPI2_MISO	Input	VCC_IO
231		SPI2_MOSI	Output	VCC_IO
233		SPI2_CS	Output	VCC_IO
235		SPI2_CLK	Output	VCC_IO
237	Digital RGB	GND	Power	GND

239		BKL1_PWM	Output	VCC_IO
241		GND	Power	GND
243		LCD1_PCLK	Output	VCC_IO
245		LCD1_VSYNC	Output	VCC_IO
247		LCD1_HSYNC	Output	VCC_IO
249		LCD1_DE	Output	VCC_IO
251		LCD1_R0	Output	VCC_IO
253		LCD1_R1	Output	VCC_IO
255		LCD1_R2	Output	VCC_IO
257		LCD1_R3	Output	VCC_IO
259		LCD1_R4	Output	VCC_IO
261		LCD1_R5	Output	VCC_IO
263		LCD1_R6	Output	VCC_IO
265		LCD1_R7	Output	VCC_IO
267		GND	Power	GND
269		LCD1_G0	Output	VCC_IO
271		LCD1_G1	Output	VCC_IO
273		LCD1_G2	Output	VCC_IO
275		LCD1_G3	Output	VCC_IO
277		LCD1_G4	Output	VCC_IO
279		LCD1_G5	Output	VCC_IO
281		LCD1_G6	Output	VCC_IO
283		LCD1_G7	Output	VCC_IO
285		GND	Power	GND
287		LCD1_B0	Output	VCC_IO
289		LCD1_B1	Output	VCC_IO
291		LCD1_B2	Output	VCC_IO
293		LCD1_B3	Output	VCC_IO
295		LCD1_B4	Output	VCC_IO
297		LCD1_B5	Output	VCC_IO
299		LCD1_B6	Output	VCC_IO
301		LCD1_B7	Output	VCC_IO
303	Analogue and Touch	AGND	Power	AGND
305		AN1_ADC0	Analogue Input	AVCC_IO
307		AN1_ADC1	Analogue Input	AVCC_IO
309		AN1_ADC2	Analogue Input	AVCC_IO
311		AN1_TSWIP_ADC3	Analogue Input	AVCC_IO
313		AGND	Power	AGND
315		AN1_TSPX	Analogue Input	N/A
317		AN1_TSMX	Analogue Input	N/A
319		AN1_TSPY	Analogue Input	N/A
321		AN1_TSMY	Analogue Input	N/A

8. Appendix C - Physical Pin Definition and Location

Signal Group	Module Bottom Side	MXM3 Pins		Module Top Side	Signal Group
GPIO	GPIO1	1	2	PWM1	PWM
	GPIO2	3	4	PWM2	
	GPIO3	5	6	PWM3	
	GPIO4	7	8	PWM4	
	GND	9	10	VCC	CAN
	GPIO5	11	12	CAN1_RX	
	GPIO6	13	14	CAN1_TX	
	GPIO7	15	16	CAN2_RX	
	GPIO8	17	18	CAN2_TX	
SATA	GND	23	24	POWER_ENABLE_MOCI	System Control
	SATA1_RX+	25	26	RESET_MOCI#	
	SATA1_RX-	27	28	RESET_MICO#	
	GND	29	30	VCC	Gigabit Ethernet
	SATA1_TX-	31	32	ETH1_MDI2+	
	SATA1_TX+	33	34	ETH1_MDI2-	
	SATA1_ACT#	35	36	VCC	
	WAKE1_MICO#	37	38	ETH1_MDI3+	
PCI-Express	GND	39	40	ETH1_MDI3-	
	PCIE1_RX-	41	42	ETH1_ACT	
	PCIE1_RX+	43	44	ETH1_LINK	
	GND	45	46	ETH1_CTREF	
	PCIE1_TX-	47	48	ETH1_MDI0-	
	PCIE1_TX+	49	50	ETH1_MDI0+	
	GND	51	52	VCC	
	PCIE1_CLK-	53	54	ETH1_MDI1-	
	PCIE1_CLK+	55	56	ETH1_MDI1+	
Reserved for type-specific features	GND	57	58	VCC	USB
	TS_DIFF1-	59	60	USBO1_VBUS	
	TS_DIFF1+	61	62	USBO1_SSRX+	
	TS_1	63	64	USBO1_SSRX-	
	TS_DIFF2-	65	66	VCC	
	TS_DIFF2+	67	68	USBO1_SSTX+	
	GND	69	70	USBO1_SSTX-	
	TS_DIFF3-	71	72	USBO1_ID	
	TS_DIFF3+	73	74	USBO1_D+	
	GND	75	76	USBO1_D-	
	TS_DIFF4-	77	78	VCC	
	TS_DIFF4+	79	80	USBH2_D+	
	GND	81	82	USBH2_D-	
	TS_DIFF5-	83	84	USBH_EN	
	TS_DIFF5+	85	86	USBH3_D+	
	TS_2	87	88	USBH3_D-	
	TS_DIFF6-	89	90	VCC	
	TS_DIFF6+	91	92	USBH4_SSRX-	
	GND	93	94	USBH4_SSRX+	
	TS_DIFF7-	95	96	USBH_OC#	
	TS_DIFF7+	97	98	USBH4_D+	
	TS_3	99	100	USBH4_D-	
	TS_DIFF8-	101	102	VCC	
	TS_DIFF8+	103	104	USBH4_SSTX-	
	GND	105	106	USBH4_SSTX+	
	TS_DIFF9-	107	108	VCC	UART

	TS_DIFF9+	109	110	UART1_DTR	
	GND	111	112	UART1_TXD	
	TS_DIFF10-	113	114	UART1_RTS	
	TS_DIFF10+	115	116	UART1_CTS	
	GND	117	118	UART1_RXD	
	TS_DIFF11-	119	120	UART1_DSR	
	TS_DIFF11+	121	122	UART1_RI	
	TS_4	123	124	UART1_DCD	
	TS_DIFF12-	125	126	UART2_TXD	
	TS_DIFF12+	127	128	UART2_RTS	
	GND	129	130	UART2_CTS	
	TS_DIFF13-	131	132	UART2_RXD	
	TS_DIFF13+	133	134	UART3_TXD	
	TS_5	135	136	UART3_RXD	
	TS_DIFF14-	137	138	UART4_TXD	
	TS_DIFF14+	139	140	UART4_RXD	
	GND	141	142	GND	
	TS_DIFF15-	143	144	MMC1_D2	
	TS_DIFF15+	145	146	MMC1_D3	
	GND	147	148	MMC1_D4	
	TS_DIFF16-	149	150	MMC1_CMD	
	TS_DIFF16+	151	152	MMC1_D5	MMC
	GND	153	154	MMC1_CLK	
	TS_DIFF17-	155	156	MMC1_D6	
	TS_DIFF17+	157	158	MMC1_D7	
	TS_6	159	160	MMC1_D0	
	TS_DIFF18-	161	162	MMC1_D1	
	TS_DIFF18+	163	164	MMC1_CD#	
	GND	165			
Parallel Camera	CAM1_D7	173	174	VCC_BACKUP	
	CAM1_D6	175	176	SD1_D2	
	CAM1_D5	177	178	SD1_D3	
	CAM1_D4	179	180	SD1_CMD	
	CAM1_D3	181	182	GND	SDIO
	CAM1_D2	183	184	SD1_CLK	
	CAM1_D1	185	186	SD1_D0	
	CAM1_D0	187	188	SD1_D1	
	GND	189	190	SD1_CD#	
	CAM1_PCLK	191	192	GND	
	CAM1_MCLK	193	194	DAP1_MCLK	
	CAM1_VSYNC	195	196	DAP1_D_OUT	
	CAM1_HSYNC	197	198	DAP1_RESET#	Digital Audio
I2C	GND	199	200	DAP1_BIT_CLK	
	I2C3_SDA	201	202	DAP1_D_IN	
	I2C3_SCL	203	204	DAP1_SYNC	
	I2C2_SDA	205	206	GND	
	I2C2_SCL	207	208	VGA1_R	
	I2C1_SDA	209	210	VGA1_G	VGA
	I2C1_SCL	211	212	VGA1_B	
SPDIF	GND	213	214	VGA1_HSYNC	
	SPDIF1_OUT	215	216	VGA1_VSYNC	
	SPDIF1_IN	217	218	GND	
SPI	GND	219	220	HDMI1_CEC	
	SPI1_CLK	221	222	HDMI1_TXD2+	HDMI
	SPI1_MISO	223	224	HDMI1_TXD2-	
	SPI1_MOSI	225	226	GND	

	SPI1_CS	227	228	HDMI1_TXD1+	
	SPI2_MISO	229	230	HDMI1_TXD1-	
	SPI2_MOSI	231	232	HDMI1_HPD	
	SPI2_CS	233	234	HDMI1_TXD0+	
	SPI2_CLK	235	236	HDMI1_TXD0-	
Digital RGB	GND	237	238	GND	Dual Channel LVDS
	BKL1_PWM	239	240	HDMI1_TXC+	
	GND	241	242	HDMI1_TXC-	
	LCD1_PCLK	243	244	GND	
	LCD1_VSYNC	245	246	LVDS1_A_CLK-	
	LCD1_HSYNC	247	248	LVDS1_A_CLK+	
	LCD1_DE	249	250	GND	
	LCD1_R0	251	252	LVDS1_A_TX0-	
	LCD1_R1	253	254	LVDS1_A_TX0+	
	LCD1_R2	255	256	GND	
	LCD1_R3	257	258	LVDS1_A_TX1-	
	LCD1_R4	259	260	LVDS1_A_TX1+	
	LCD1_R5	261	262	USBO1_OC#	
	LCD1_R6	263	264	LVDS1_A_TX2-	
	LCD1_R7	265	266	LVDS1_A_TX2+	
	GND	267	268	GND	
	LCD1_G0	269	270	LVDS1_A_TX3-	
	LCD1_G1	271	272	LVDS1_A_TX3+	
	LCD1_G2	273	274	USBO1_EN	
	LCD1_G3	275	276	LVDS1_B_CLK-	
	LCD1_G4	277	278	LVDS1_B_CLK+	
	LCD1_G5	279	280	GND	
	LCD1_G6	281	282	LVDS1_B_TX0-	
	LCD1_G7	283	284	LVDS1_B_TX0+	
	GND	285	286	BKL1_ON	
	LCD1_B0	287	288	LVDS1_B_TX1-	
	LCD1_B1	289	290	LVDS1_B_TX1+	
	LCD1_B2	291	292	GND	
	LCD1_B3	293	294	LVDS1_B_TX2-	
	LCD1_B4	295	296	LVDS1_B_TX2+	
	LCD1_B5	297	298	GND	
	LCD1_B6	299	300	LVDS1_B_TX3-	
	LCD1_B7	301	302	LVDS1_B_TX3+	
Analogue and Touch	AGND	303	304	AGND	Analogue Audio
	AN1_ADC0	305	306	AAP1_MICIN	
	AN1_ADC1	307	308	AGND	
	AN1_ADC2	309	310	AAP1_LIN_L	
	AN1_TSWIP_ADC3	311	312	AAP1_LIN_R	
	AGND	313	314	AVCC	
	AN1_TSPX	315	316	AAP1_HP_L	
	AN1_TSMX	317	318	AAP1_HP_R	
	AN1_TSPY	319	320	AVCC	
	AN1_TSMY	321			